

Amber FX Statistical Static Timing Analyzer

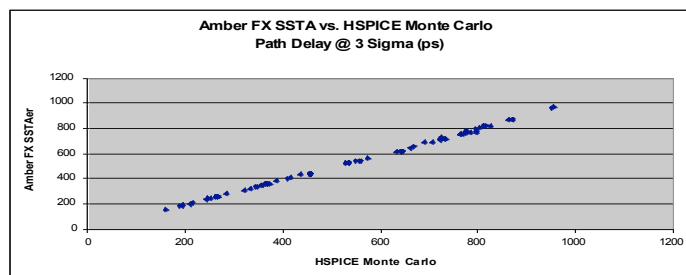
Amber™ FX SSTA is a path based statistical static timing analyzer that delivers near SPICE accuracy combined with the threaded performance and capacity of the Amber™ Static Analysis tool suite. Amber FX SSTA integrates statistical static timing analysis (SSTA) with high accuracy transistor models that can be generated in hours using the latest process data from semiconductor foundries. Chip designers can now validate the performance and margins of leading-edge designs with more accurate statistical analysis and the most current manufacturing information right up to tape-out. Amber FX Transistor SSTA is supported in the TSMC Reference Flow 9.0.

Amber FX SSTA can work with any STA tool, including Amber STA or other industry offerings.

Manufacturing variance is one of the biggest barriers to successful adoption of advanced 45-nm and 40-nm process nodes. Although the expectation is that these nodes will deliver much better speed and power at a lower cost per die, traditional corner-based timing closure methodologies are much too pessimistic and make timing closure very difficult. Statistical timing tools and new library formats such as CCSM and ECSM are supposed to address these problems. However, these tools and models are slower than their predecessors, and generating libraries can take weeks causing them to be out of sync with the latest foundry data. It may be very difficult to obtain CCS or ECSM libraries for third party IP or legacy blocks, making it impossible to deploy SSTA.

Amber FX SSTA removes these barriers with a FX transistor model that captures delay and variance directly from SPICE, the foundry SPICE model, and the SPICE netlists for each of the cells. The Amber FXM library is a cell-level library that includes all of the transistors and

parasitics for each cell. Amber FXM has been qualified with TSMC 65-nm and 40-nm libraries using Berkeley SPICE and HSPICE™ for characterization. FXM is an extension to the Liberty format and addresses a large number of known accuracy problems in existing Liberty, ECSM, and CCSM libraries. It handles a wide range of high-risk timing behaviors that are not properly modeled by other timing solutions, such as multiple input switching, non-linear input slopes, voltage drop, functional noise, etc.



Amber FX Transistor SSTA is used for path-based TSSTA with the FXM model. Corners are replaced with a statistical distribution for the timing, which represents the potential manufacturing variance as tracked and analyzed by the foundry. Users first complete a baseline static timing run, and then select a set of paths for full transistor-level SSTA. The nominal delay and variance of these paths is then recalculated using the FXM model and delay calculator. For the purposes of reporting, delay is now reported as the mean or nominal, plus a delta for variance, usually 3σ .

Amber FX SSTA addresses known limitations in the current static and statistical analysis flow:

1. **Corner Pessimism:** Amber FX SSTA addresses the inherent pessimism of corner-based timing at advanced process nodes. Amber SSTA provides an alternative way to evaluate failing paths and timing slack.
2. **Accuracy:** Amber FX SSTA is within 2% of SPICE for both delay and variance.
3. **Model availability:** FX models are derived directly from the SPICE libraries for cells, and be characterized in a matter of hours. Libraries can be easily kept up to date with the latest process parameters from the fab.
4. **Performance:** With its path based approach, and threaded processing, Amber FX SSTA can evaluate entire designs faster than other tools can do STA.
5. **Capacity:** Amber FX SSTA can be used at the full chip level, unlike other tools that only operate at the block level.
6. **Flow Compatibility:** Amber FX SSTA can be used with any STA tool. Users can identify paths of interest with their existing STA tools, and then they can be evaluated in Amber FX SSTA. Users can now adopt high accuracy SSTA with a minimum amount of disruption to their existing flow and methodology.

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